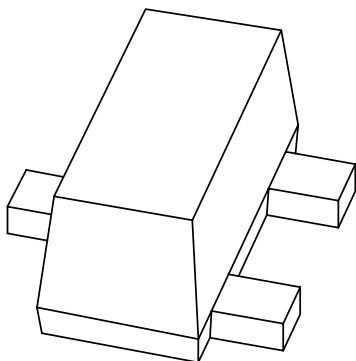


# DATA SHEET



## **PDTTC144WEF**

**NPN resistor-equipped transistor;  
R1 = 47 k $\Omega$ , R2 = 22 k $\Omega$**

Product specification

2002 Mar 14

**NPN resistor-equipped transistor;**  
**R1 = 47 kΩ, R2 = 22 kΩ**

**PDTC144WEF**

**FEATURES**

- Built-in bias resistors
- 250 mW total power dissipation
- Very small 1.6 × 0.85 mm thin package
- Flat leads
- Excellent coplanarity
- Improved thermal behaviour
- Reduces number of components and required PCB area.

**APPLICATIONS**

- General purpose switching and amplification
- Inverter and interface circuits
- Driver circuits.

**DESCRIPTION**

NPN resistor-equipped transistor in a SOT490 (SC-89) plastic package.

**MARKING**

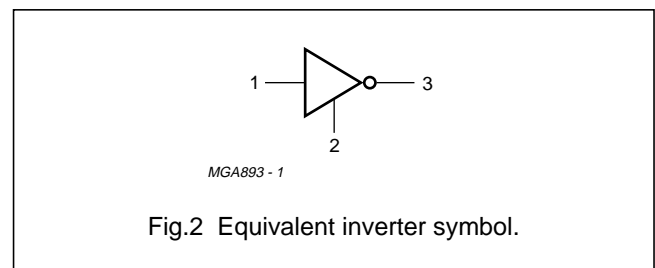
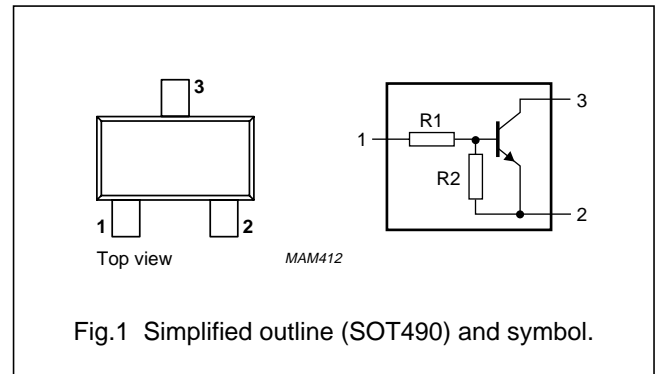
TYPE NUMBER	MARKING CODE
PDTC144WEF	34

**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	MAX.	UNIT
V <sub>CEO</sub>	collector-emitter voltage	50	V
I <sub>O</sub>	output current (DC)	100	mA
R1	bias resistor	47	kΩ
R2	bias resistor	22	kΩ

**PINNING**

PIN	DESCRIPTION
1	base/input
2	emitter/ground (+)
3	collector/output



NPN resistor-equipped transistor;  
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PDTC144WEF

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CB0</sub>	collector-base voltage	open emitter	–	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base	–	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector	–	10	V
V <sub>i</sub>	input voltage				
	positive		–	+40	V
	negative		–	–10	V
I <sub>o</sub>	output current (DC)		–	100	mA
I <sub>CM</sub>	peak collector current		–	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C; note 1	–	250	mW
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>amb</sub>	operating ambient temperature		–65	+150	°C

**Note**1. For mounting conditions, see “*Thermal considerations and footprint design for SOT490 in the SC18 Data Handbook*”.**THERMAL CHARACTERISTICS**

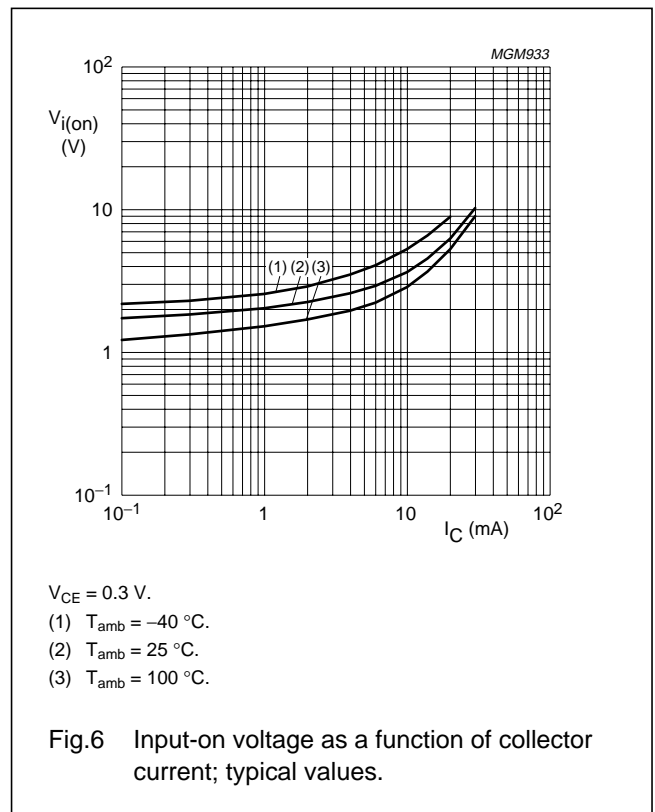
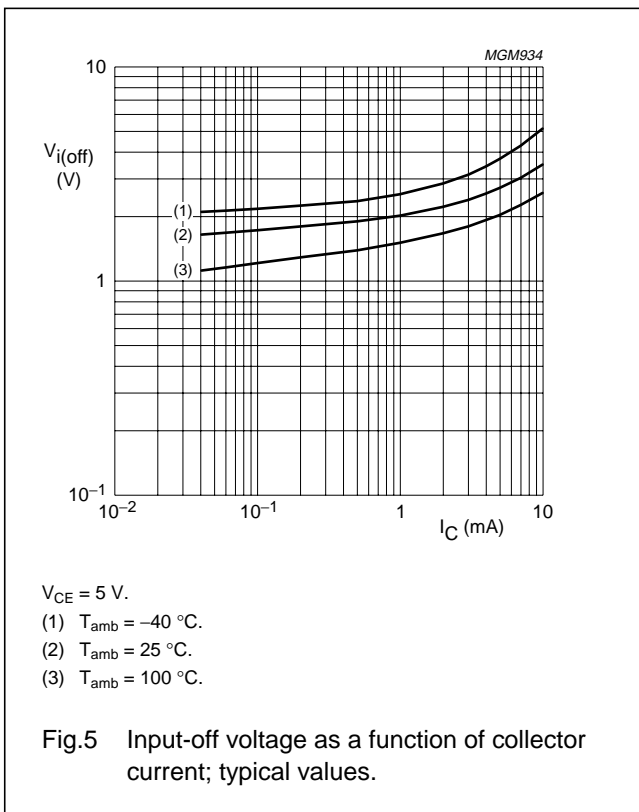
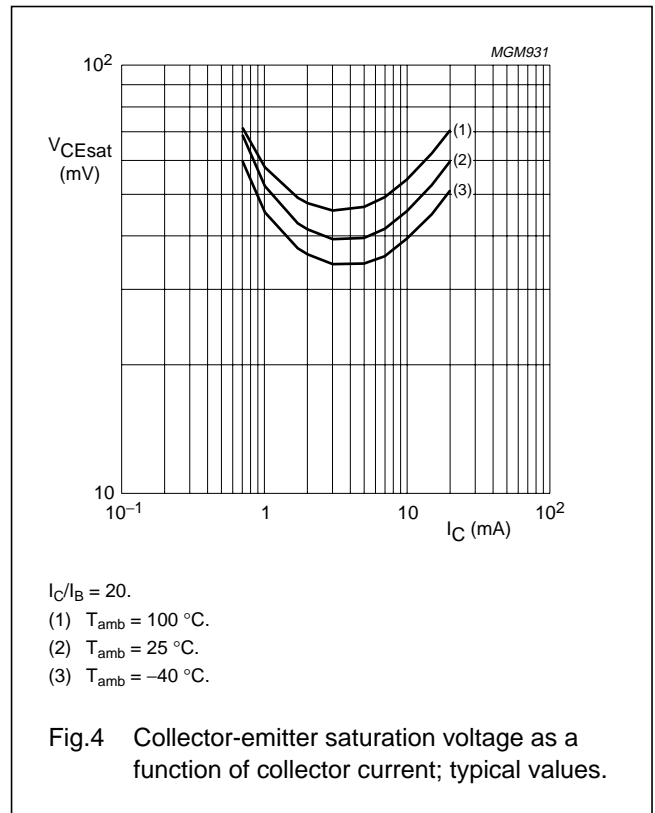
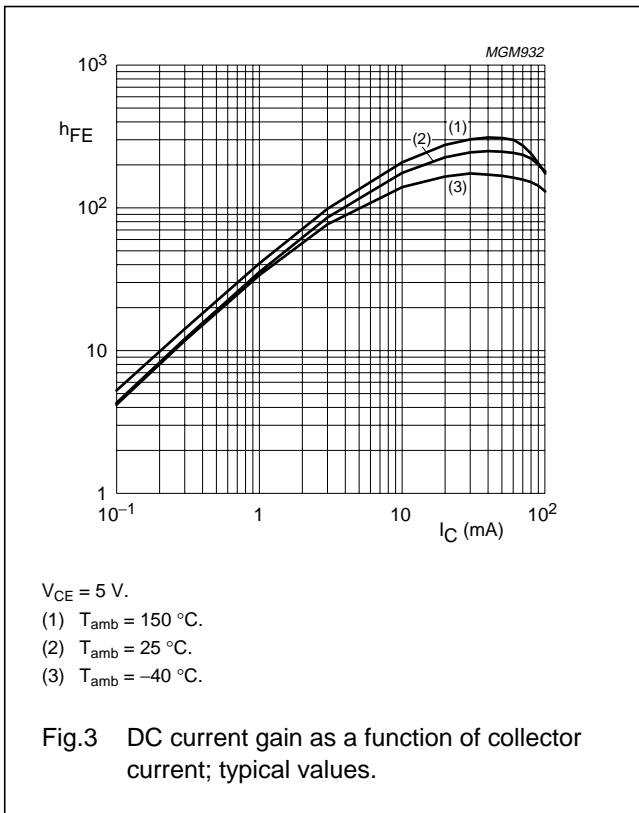
SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th j-a</sub>	thermal resistance from junction to ambient	in free air; note 1	500	K/W

**Note**1. For mounting conditions, see “*Thermal considerations and footprint design for SOT490 in the SC18 Data Handbook*”.**CHARACTERISTICS**T<sub>amb</sub> = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = 50 V; I <sub>E</sub> = 0	–	–	100	nA
I <sub>CEO</sub>	collector-emitter cut-off current	V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0	–	–	1	μA
		V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0; T <sub>j</sub> = 150 °C	–	–	50	μA
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = 5 V; I <sub>C</sub> = 0	–	–	110	μA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 5 mA	60	–	–	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = 10 mA; I <sub>B</sub> = 0.5 mA	–	–	150	mV
V <sub>i(off)</sub>	input off voltage	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 100 μA	–	1.7	1.2	V
V <sub>i(on)</sub>	input on voltage	V <sub>CE</sub> = 0.3 V; I <sub>C</sub> = 2 mA	4	2.7	–	V
R1	input resistor		33	47	61	k $\Omega$
$\frac{R2}{R1}$	resistor ratio		0.37	0.47	0.57	
C <sub>c</sub>	collector capacitance	I <sub>E</sub> = i <sub>e</sub> = 0; V <sub>CB</sub> = 10 V; f = 1 MHz	–	–	2.5	pF

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PDTC144WEF



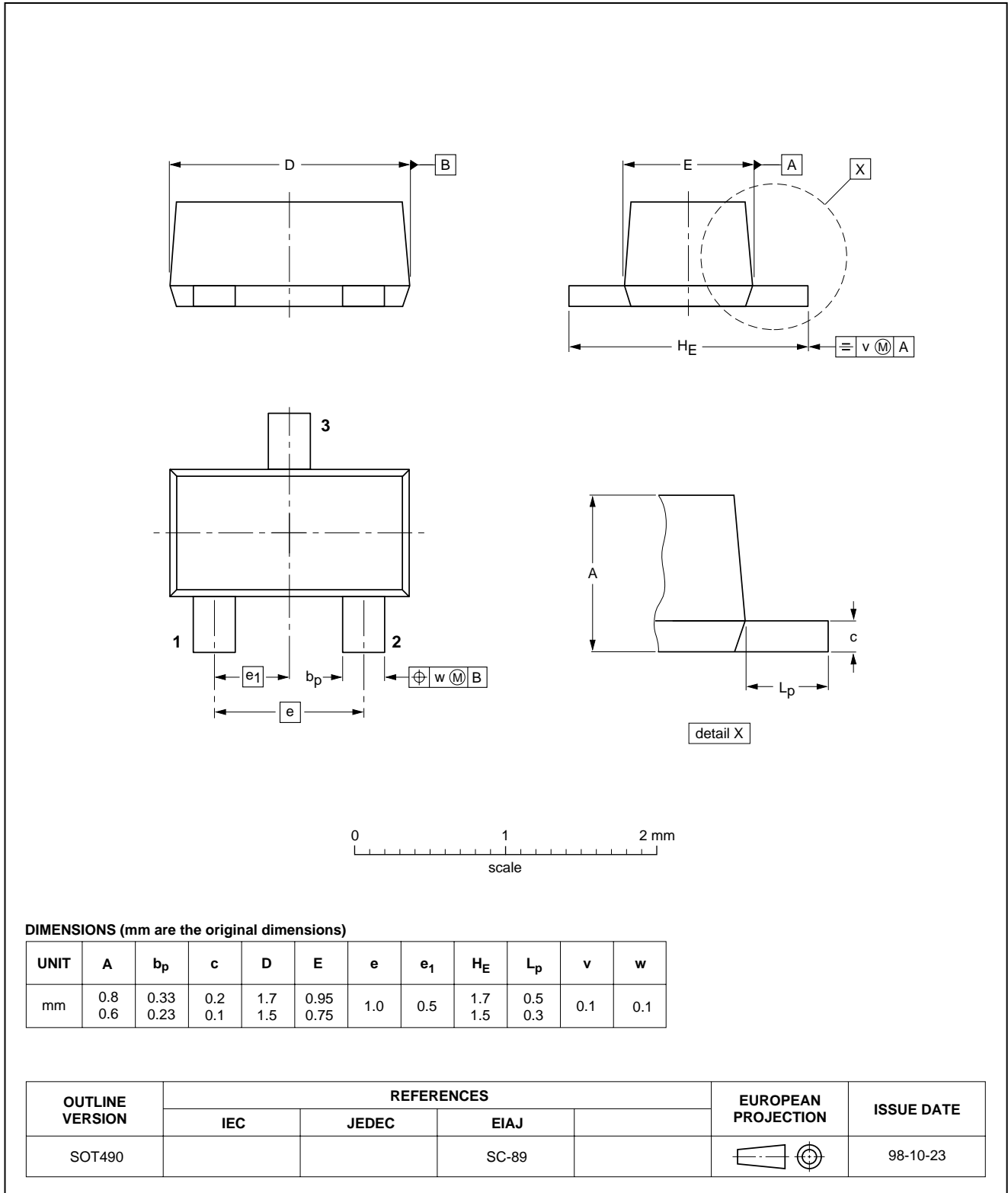
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PDTC144WEF

PACKAGE OUTLINE

Plastic surface mounted package; 3 leads

SOT490



NPN resistor-equipped transistor;  
R1 = 47 k $\Omega$ , R2 = 22 k $\Omega$

PDTC144WEF

#### DATA SHEET STATUS

DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITIONS
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PDTC144WEF

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**NOTES**

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